
LIST OF EXPERIMENTS
SUBJECT: Digital Techniques Lab
Branch – Information Technology, II Sem

1. To study and verify Basic Logic gates (AND,OR,Not).
2. To study and verify Universal gates (NAND,NOR).
3. To study and verify the operation of half adder and Full adder.
4. To study and verify the operation of Full adder.
5. To verify the operation of BCD Decoder.
6. Design and verify the operation of the RS Flip Flop.
7. Design and verify the operation of the JK and D Flip Flop.
8. To display one digit BCD number on Seven-segment Display.

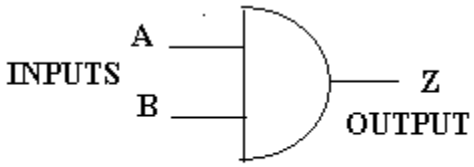
EXPERIMENT NO: 01

1. **AIM: -** To study and verify Basic Logic gates (AND, OR, NOT).

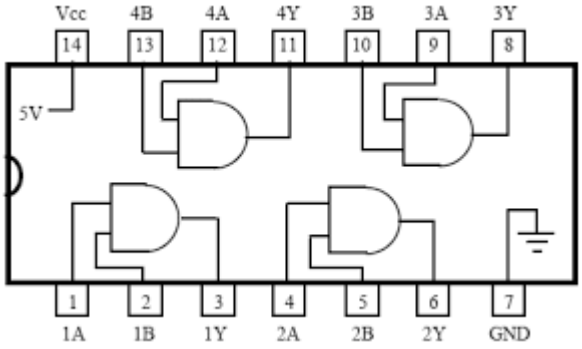
2. **APPRATUS REQURIED: -B**read board, connecting leads,LEDs,IC7408,IC7432,IC7402,IC7400,IC74135,Resistors,9vBattery

3. **THEORY: -** The various logic gates are as follows:
   AND GATE: - The AND gate performs logical multiplication. AND gate Circuit has two inputs and one output. Whenever both the inputs are high Or 1 the output for this will be logic high or 1and low otherwise. The truth Table for AND gate is:

INPUTS		OUTPUT
A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1



AND Gate

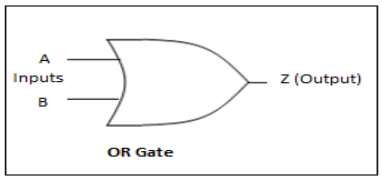


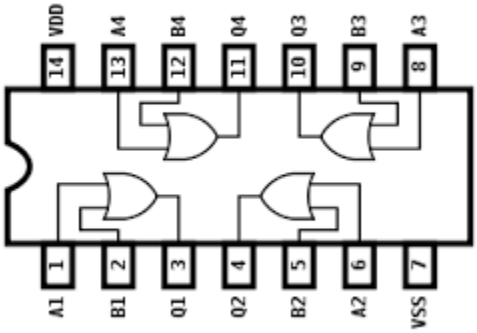
IC7408

OR GATE: -The OR gate performs logical addition. OR gate ckt has two inputs and one output. Whenever both the inputs are low or 0 the output for this will be logic low or 0 and high or 1 otherwise. The truth table for OR gate is

INPUTS	OUTPUT

A	B	Z
0	0	0
0	1	1
1	0	1
1	1	1

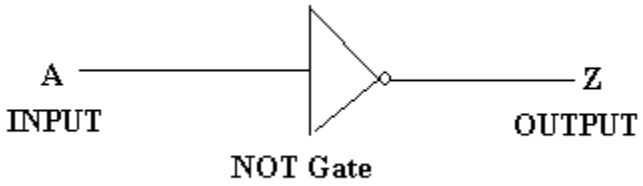




IC 7432

NOT GATE: - The inverter (Not Circuit) performs a basic logic function called inversion or complementation. This gate has only one input and one output. NOT gate is called the inverter because output state is always opposite to the input state. When the input is low or 0, the output is logic high or 1 and vice versa.

INPUT	OUTPUT
0	1
1	0



4. **PROCEDURE**: Using Bread Board:

- Connect the circuit as per circuit diagrams one by one.
- Connect the input terminal to the input pins of IC.
- Connect the output terminal to the logic indicator LED.
- To Pin no 7 connect the ground and to pin no 14 connect the +5V Vcc supply.
- Verify the Truth Tables of various logic gates.

5. **Result:** The Operation of Logic Gate is successfully verified.

EXPERIMENT NO: -02

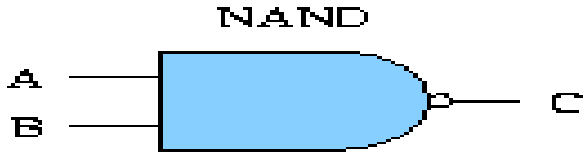
1. **AIM: -** To study and verify Universal gates (NAND, NOR).

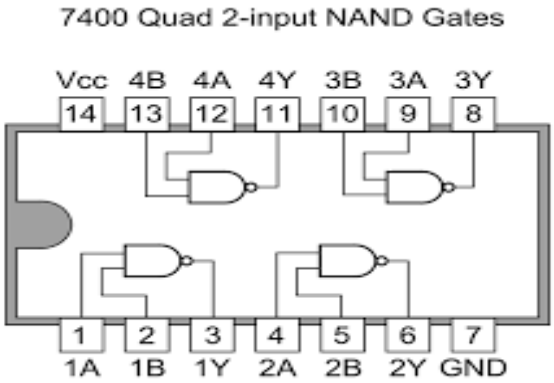
2. **APPRATUS REQURIED: -B**read board, connecting leads,LEDs,IC7408,IC7432,IC7402,IC7400,IC74135,Resistors,9vBattery

3. **THEORY: -** The various logic gates are as follows:

NAND GATE:- The term NAND is a contraction of NOT –AND and implies an AND function with complemented output. NAND gate has two inputs and one output. Whenever at least one of the inputs is low, the output voltage will be high. If both inputs are high, then the output logic is low. The truth table for NAND gate is:

INPUT		OUTPUT
A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

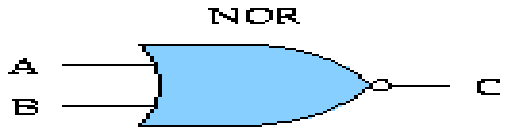


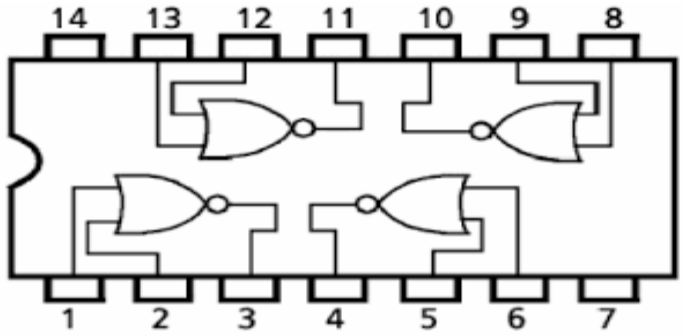


NOR GATE:- The term NOR is a contraction of NOT –NOR and implies an OR function with an inverted output. The circuit has two inputs and one output. Whenever at least one of the

inputs is high or 1, the output will be low or 0 .If both inputs are low, then output is high or 1.The truth table for NOR gate is:

INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0





IC-74135

1. **PROCEDURE**: Using Bread Board:

- Connect the circuit as per circuit diagrams one by one.
- Connect the input terminal to the input pins of IC.
- Connect the output terminal to the logic indicator LED.
- To Pin no 7 connect the ground and to pin no 14 connect the +5V Vcc supply.
- Verify the Truth Tables of various logic gates.

4. **Result:** The Operation of Logic Gate is successfully verified.

EXPERIMENT NO: -03

1. **AIM: -** To study and verify ExOR and ExNOR gates

2. **APPRATUS REQURIED: -B**read board, connecting leads,LEDs,IC7408,IC7432,IC7402,IC7400,IC74135,Resistors,9vBattery

3. **THEORY: -** The various logic gates are as follows:

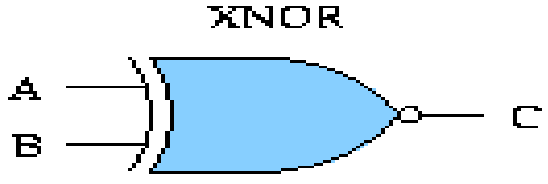
EX- OR GATE:- EX-OR gate circuit has two inputs and one output. Whenever both the inputs are the same, the corresponding output will be low otherwise the output will be logic high or 1.The truth table for EX-OR gate is :

INPUT		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XOR Gate

ExNOR GATE:- EXNOR gate circuit has two inputs and one output. Whenever both the inputs are same, the output will be logic high or 1 otherwise output will be logic low. The truth table for EXNOR gate is:

INPUT		OUTPUT
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1



4. **PROCEDURE**: Using Bread Board:

- Connect the circuit as per circuit diagrams one by one.
- Connect the input terminal to the input pins of IC.
- Connect the output terminal to the logic indicator LED.
- To Pin no 7 connect the ground and to pin no 14 connect the +5V Vcc supply.
- Verify the Truth Tables of various logic gates.

5. **Result:** The Operation of ExOR and ExNOR gates is successfully verified.

EXPERIMENT NO.- 04

1. **AIM: -** Design and verify the operation of Half Adder and Full Adder.

2. **APPRATUS REQUIRED: -** Bread Board, EX-OR Gate IC-7486, OR Gate IC-7432, AND Gate IC – 7408, and Connecting leads or Hookup wires, color LEDs.

3. **THEORY: -**

HALF ADDER: - It is combinational circuits that perform addition of two bits. This circuit has two inputs A and B (augends and added) and two outputs- Sum (S) and Carry (C).The sum is a 1 when A and B are different and carry is a 1when A and B are 1.The truth table for a half adder can be constructed using the addition table for binary numbers,

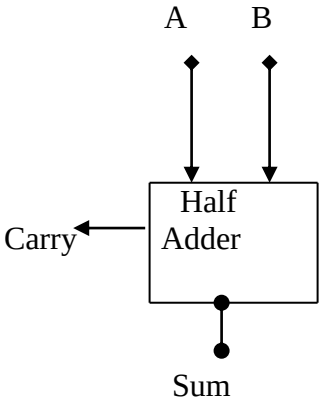
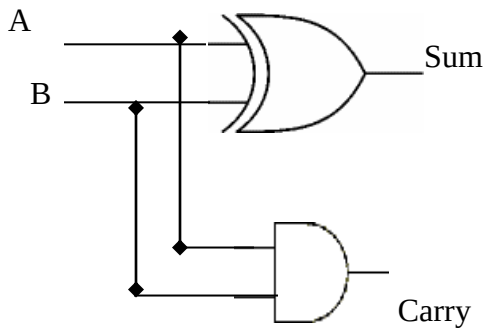


Fig: - (a) Functional diagram of Half Adder (b) Truth Table.

From the truth table, we can write logical expression for S and C outputs as

$$S = A\overline{B} + \overline{A}B$$
$$C = AB$$

Implementation of Half Adder: - Half Adder the sum is implemented using XOR gate while carry is implemented using AND gate.



Truth Table of Half Adder

INPUT		OUTPUT	
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	1	1

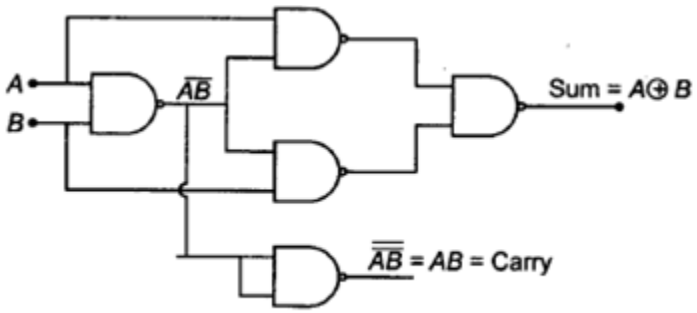
FULL ADDER: - Half adder can only add two inputs and has no provision to add carry coming from the lower order bits when multiple additions is performed. For this purpose a third input terminal is added and this circuit is used to add augend, addend and carry generated from previous addition. The full adder is a combinational circuit that performs sum of three inputs bits. This circuit has three inputs and two outputs. Two of the inputs, denoted by A and B, represent the two bits to be added. The third inputs C_{in} represent the carry from the previous lower significant position. The two outputs are denoted by the symbols S for the sum and C_{out} for carry.

$$S = \bar{A}B\bar{C}_{n-1} + \bar{A}\,\bar{B}C_{n-1} + A\bar{B}\bar{C}_{n-1} + ABC_{n-1}$$

$$S = C_{n-1}(A\,\bar{B} + \bar{A}B) + \bar{C}_{n-1}(A\bar{B} + \bar{A}B)$$

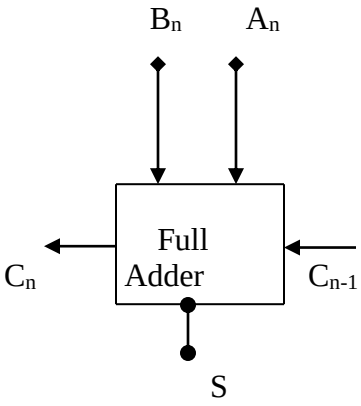
$$C_{out} = AB + AC_{n-1} + BC_{n-1}$$

Fig :(c) Implementation of Half Adder using EXOR Gate



Half adder logic diagram using NAND gate

Inputs			Outputs	
A	B	C_{n-1}	C_n	S
0	0	0	0	0



(d)

0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(e)

Fig: - (d) Functional diagram of Full Adder (e) Truth Table

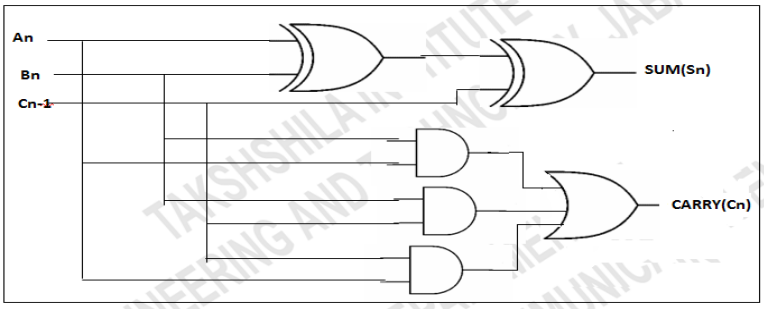


Fig: - (f) Circuit Diagram of Full ADDER.

4. PROCEDURE:-

Using Bread Board-

1. Connect the circuit as per circuit Diagram using ICs.
2. Connect the Input terminal to the Input pins of ICs.
3. Connect the Output terminal to the Logic Indicator LED.
4. Pin no. 7 are connect the Ground and Pin no. 14 connect the +5V VCC Supply.
5. Switch ON the power supply.
6. Verify the Truth Table.

5. RESULT: - Thus, we have verified the truth table of Half Adder and Full Adder.

EXPERIMENT NO. - 5

1.AIM: - To verify the operation of 4:1Multiplexer.

2. **APPRATUS REQUIRED: -** Bread Board, OR Gate IC-7432, AND Gate IC – 7408, and Hookup wires.

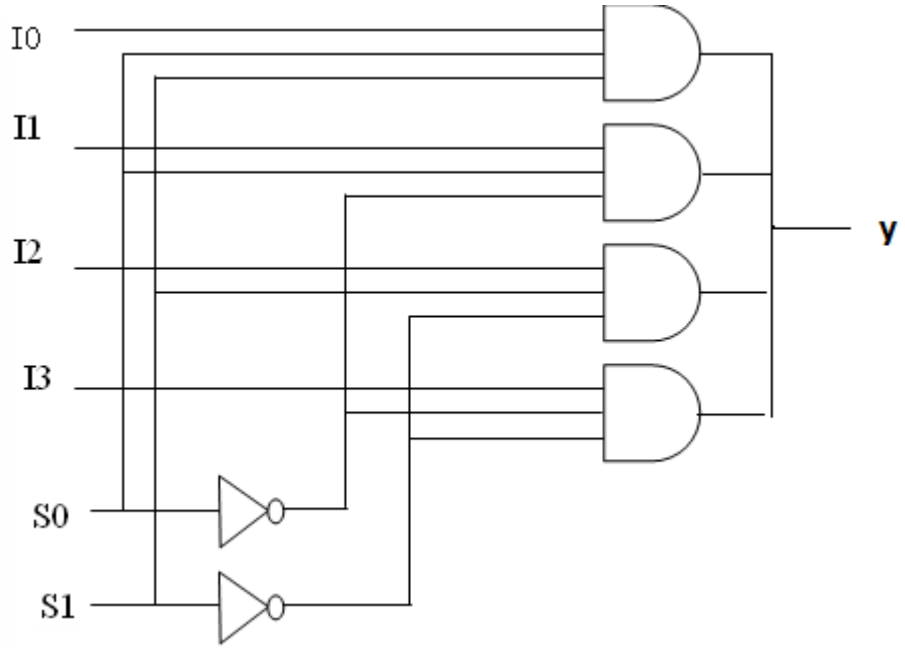
3. **THEORY: -** A multiplexer is a circuit which has a number of inputs but only 1 output or we can say multiplexer is a circuit which transmits a large number of information signals (inputs) over a small number of signal lines (output).Digital multiplexer is a combinational logic circuit and its function is to select information in binary from one of many inputs and outputs the information along a single selected output. These circuits are especially useful when a complex logic circuit is to be shared by a number of input signals. The information to be outputted is selected by the address line. In case of 4:1 multiplexer, it has four input lines having a signal as I_0, I_1, I_2 and I_3.For selecting one of the four input signals we require address which can be a two bit word. The address lines are designated as S_1 and S_0.For each combination of selection signals (S_1 and S_0) one of the inputs is outputted. The truth table for having output Y as a function of S_1 and S_0.The truth table of 4:1 Multiplexer are as follows:

S_1	S_2	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

This truth table can be expressed by the following Boolean expression.

$Y= I_0 S_1S_2 + I_1S_1S_2 + I_2S_1S_2 + I_3S_1S_2$

I_0, I_1, I_2 and I_3 are Boolean variables and will have a value of 0 or 1.A 0 will mean that particular I is 0 or it is not at the output while a 1 will mean that a particular I appears at the output. Sometimes a multiplexer works as a data selector by working as a circuit which selects one of many inputs and transmits that information along a reselected line and that is why it is also called as data selector.



4. **PROCEDURE:-**
   - Procedure for Multiplexer4:1 on breadboard as follows:-
   - Connect the Input terminal of the circuit to the Input logic.
   - Connect the Output terminal to LED.
   - Switch ON the power supply.
   - Verify the Truth Table.

5. **RESULT: -** Thus, we have verified the operation of 4:1 multiplexer.

EXPERIMENT NO.-06

1. **AIM: -** To verify operation of BCD decoder.

2. **APPARATUS REQUIRED-**
Trainer kit or bread board, AND gate IC 7408, NOT gate IC 7404, +5 V power supply & connecting leads or hookup wires.

3. **THEORY –**
A decoder is a logic ckt that converts an n bit binary I/P code into 2^n O/P lines such that each O/P line will be activated for only possible combination of I/P in a decoder. No. of O/Ps is greater than no. of I/Ps. Decoding is necessary in applications such as data multiplexing, digital displays, D to A converter and memory addressing.
A decoder that takes a 4 bit BCD as I/P code and produces 10 O/Ps corresponding to decimal digits is called a BCD to decimal decoder. Hence each O/P goes high when its corresponding BCD code is applied at I/P.

Table:-

D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0

WHERE 1 = HIGH LEVEL
0 = LOW LEVEL

4. **PROCEDURE-**
Procedure for BCD to decimal decoder on trainer kit,
1. 1-Connect I/P terminal of ckt to I/P logic.
2. 2-Connect O/P terminal to logic indicator.
3. 3-Switch ON power supply.
4. 4-Verify the truth table.

Using bread board

1. Connect circuit as per diagram.
2. Connect I/P terminal to I/P pins of IC.
3. Connect O/P terminal to logic indicator.

4. Pin no. 7 is connected to ground & pin no. 14 is connected to +5 V supply.
5. Switch on power supply.
6. Verify the truth table.

5. **RESULT:-**Thus we have verified truth table of BCD to decimal decoder.

EXPERIMENT NO.-07

1. **AIM:** - To verify the operation of JK and D flip –flop.

2. **APPARATUS REQUIRED-**
   Trainer kit method: - Trainer kit, connecting leads.
   Bread board method: - Bread board, hookup wires, JKfilp flop IC 7473,D flip flop IC 7474 connecting leads, hookup wires.

3. **THEORY –F**lip flop is the simplest type of sequential circuit .It is a memory cell that has only two states. it can be either 1 or 0 .such two state sequential circuit are called Flip-flop because they flip from one state to another and then flop back .a flip flop is also known as multivariate ,latch . In case of flip flop there are one or more inputs and two outputs Q and Q. the two outputs are complementary to each other, if Q=0 then $\bar{Q}$ =1 .When the flip flop output Q=0 or 1 ,it will remain in that stable state until one or more of the input are executed to effect a change in the o/p since the flip flop o/p will remain set /reset until the trigger pulse is given to change the state . It can be regarded changes their

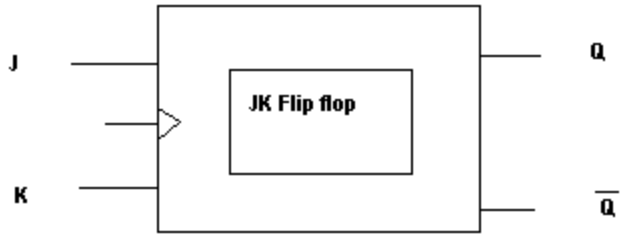
As a memory device to store one binary digit. these synchronous sequential circuit changes their state when the clock pulses are present .

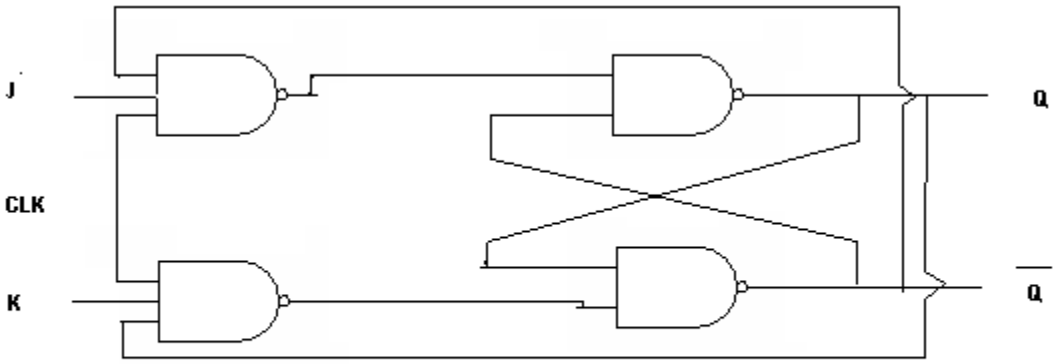
JK flip-flop:

This flipflop is having two data input J and k flip flop and two outputs Q and Q. this flip flop change s their state when the clock pulses are present. In case of JK flipflop the truth table are as follows:

1. If J =0, K=0 then there is change in the previous states or o/p.
2. If J =0, K=1 then the o/p Q=0 then Q =1. It's called clear condition of flipflop.
3. If J =1, K=0 then the o/p Q=0 then Q =1 is. It's called set condition of flipflop.
4. If J =1, K=1 then the flipflop is in toggle mode. Toggle mode is that the flipflop. will give the complement o/p of the previous state.

INPUT		OUTPUT	ACTION
J	K	Qn+1	
0	0	Qn	No change
0	1	Q	Reset
1	0	1	Set
1	1	$\bar{Q}$n	Toggle





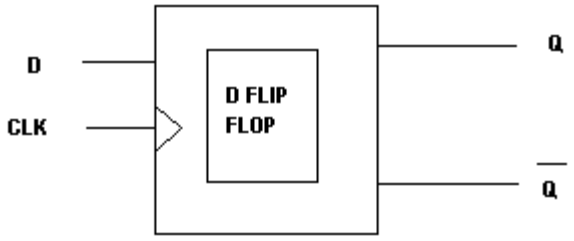
Logic Diagram Of JK FLIPFLOP

D FLIPFLOP: -This flipflop is having one data i/p Dand two Q. $\overline{}$ This flip flop changes their state when the state when the clock pulses are present. In case of D flip flop the truth table are as follows:

1. If D= 0 then the O/P Q=0 and Q=1. It's called clear condition of flipflop.
2. If D=1 then the O/P Q=1 and Q=0 .Its called set condition of flipflop.

The truth table of D FLIPFLOP is as follows:

input	OUTPUT	ACTION
D	Qn+1	
0	0	Reset
1	1	Set



4 PROCEDURE: Using Bread Board:

- Connect the circuit as per circuit diagrams one by one.
- Connect the input terminal to the input pins of IC.
- Connect the output terminal to the logic indicator LED.
- To Pin no 7 connect the ground and to pin no 14 connect the +5V Vcc supply.
- Verify the Truth Tables of various logic gates.

5. **RESULT:-**Thus we have verified truth table of the operation of JK and D flip –flop.

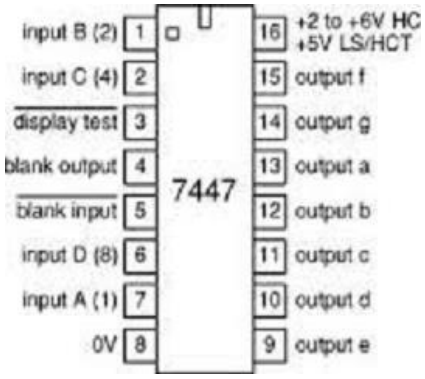
EXPERIMENT NO: -08

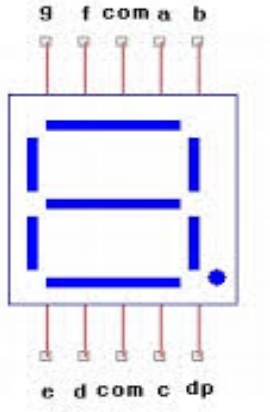
1. **AIM: -** To display one digit BCD number on Seven-segment Display

2. **APPARATUS REQURIED**: -Bread board, connecting leads, BCD to Seven-segment Display converter IC 7447, Seven-segment Display IC FND 507, Resistor 330Ω, 9vBattery

3. **THEORY:**

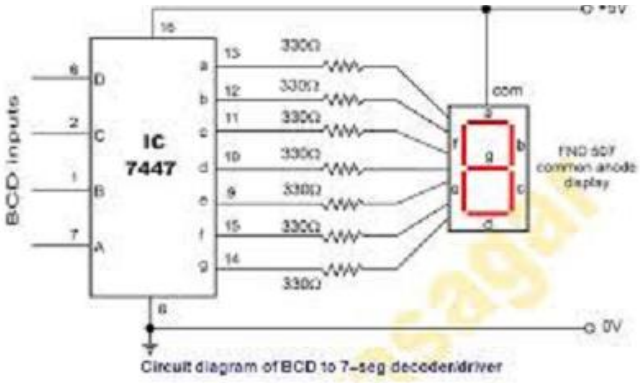
1. BCD to Seven-segment Display converter/driver IC 7447 is a 16 pin MSI Integrated Circuit(IC) which operates on TTL logic .It can sink 40ma current.
2. The V_{CC} is +5V.
3. 4-bit BCD number (DCBA) is given at input lines which are active high.
4. There are seven output lines (low active) which drive the Seven-segment Display.
5. Display test (pin3) is active low input to test all LEDs of seven segment display.
6. Blank input (pin5) is kept at logic 1 for normal display operation. It is given logic 0 input to blank out display for leading zeros in multi digit display.
7. Blank output (pin4) which is normally at logic 0, goes to logic 1 for blanking out display for leading zeros in multi digit display. It is connected to Blank input of cascaded IC 7447.
8. The Seven-segment Display IC FND 507 is a common anode display unit. There are seven LEDs arranged in letter "8". The anodes of all LEDs are commonly connected to V_{CC} is +5V. Low input is given to input line to glow corresponding LED. The pine diagrams are given below:





4. **PROCEDURE**: Using Bread Board:

- Connect the circuit as per circuit diagrams one by one.
- Connect the input terminal to the input pins of IC.
- Connect the output terminal to the logic indicator LED.
- To Pin no 7 connect the ground and to pin no 14 connect the +5V Vcc supply.
- Verify the Truth Tables of various logic gates.



Circuit diagram of BCD to 7-seg decoder/driver

5. **RESULT:** We have successfully displayed one digit number on seven segment display.